Observation of the Nonlinear Behaviour of PFC **Boost Converter and Control of Bifurcation**

Arnab Ghosh, Abhisek Pal, Dr. Pradip Kumar Saha, Dr. Gautam Kumar Panda

Abstract— With rapid development in power semiconductor devices, the usage of power electronic systems has expanded to new and wide application range that include residential, commercial, aerospace and many others. However, their non-linear behavior puts a question mark on their high efficiency. This paper aims to develop a circuit for PFC boost converter to observe chaos and bifurcation diagrams. It is clear that the output storage capacitor is a main contributing parameter on the system stability, therefore, bifurcation maps are developed to determine the accurate minimum output capacitance value that assures the system stability under all operating conditions.

Index Terms— PFC boost converter; Phase Plane Trajectories ; Bifurcation diagrams ; Bifurcation Control .

1 INTRODUCTION

^THE power electronic engineers observe some strange phenomena noise like oscillation. Actually power electronics system can exhibit a variety of nonlinear behaviours because of periodic switching of the circuits. This kind of nonlinearity is the main cause of harmonics generation i.e. degradation of input power factor. In the last decade, bifurcation and chaotic phenomena have been reported in some type of DC-DC converters [1,5,8]. Here we are discussing about some nonlinear phenomena of Power Factor Corrected (PFC) Boost Converter.

The operation of the boost PFC converter [2, 6] has been analyzed in details by many researchers. In practical circuits, it is much more difficult to arrange pure DC source, as well as the setup is much more expensive. So we are considering rectified dc in spite of pure DC.

They linearised the system as their assumption. They assumed a very huge output capacitance (not acceptable in industry) and it resulted in the time-invariant feedback signal that neglected the time-varying effect. Also, they replaced the input voltage with its root mean square (r.m.s.) value, neglecting the effect of its amplitude variation. Then, they introduced a small-signal equivalent circuit and the stability was

examined by this linear model.

The PFC converter is nonlinear system [6] due to a multiplier using and a large variation of duty cycle. There is also present nonlinear term in its state equations. Here we will observe the chaotic behaviour and bifurcations of this converter.

What is Chaos?

The etymology of the word "chaos" [7,8] is a Greek word " $\chi \alpha' \xi$ " which means "the nether abyss, or infinite darkness," Namely, the god Chaos was the foundation of all creation. There is no standard definition of chaos. The chaos has some typical features: Nonlinearity, Determinism, Sensitive dependence on initial conditions, Aperiodicity.

What is Bifurcations?

The quantitative changes of system parameters can cause of the qualitative changes of the system dynamics are called Bifurcations [7,8]. Naturally, bifurcations are very important dynamical events that may affect the performance of engineering systems.

2 PFC BOOST CONVERTER AND PROPOSED MODEL

Modelling, simulation and circuit analysis are done by MAT-LAB respectively. These not only help in developing a deeper understanding of PFC converters but are also extremely important tools for design verification and performance evaluation. These techniques help in the evaluation of a system without risking the huge cost and effort of developing and testing an actual converter.

Fig 1: Block Diagram of a boost PFC circuit

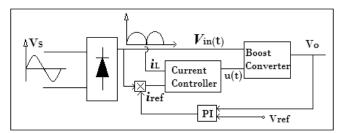
From the above Fig.1 the single phase sinusoidal voltage source v_s is rectified by diode bridge and the rippled DC voltage v_{in} is fed to the boost converter. The output voltage v_o (ripple is presented as the value of the capacitor is taken

[•] Arnab Ghosh is currently pursuing M.Tech in Power Electronics and Drives at Jalpaiguri Govt. Engineering College, India, PH-9433379717. E-mail: arnab.4u2010@gmail.com

[•] Abhisek Pal is currently pursuing M.Tech in Power Electronics and Drives at Jalpaiguri Govt. Engineering College ,India, PH-8900063865. E-mail: abhisekpal.ee @gmail.com

[•] Dr. Pradip Kumar Saha Ph.D., is Professor and Head of the Department of Electrical Engineering at Jalpaiguri Govt. Engineering College, Jalpaiguri, India, PH-9832443022. *E-mail:* p_ksaha@rediffmail.com

[•] Dr. Gautam Kumar Panda Ph.D., is Professor of the Department of Electrical Engineering at Jalpaiguri Govt. Engineering College, Jalpaiguri, India, PH-9434449763. E-mail: g_panda@rediffmail.com



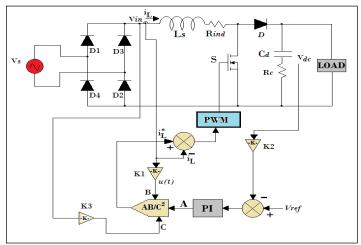
small) is obtained from load side. The output voltage v_o is compared with a reference voltage (DC) v_{ref} . We use an integral controller to get steady state value of error signal. iref is obtained after combining the the result of controller, vin and inductor current (i_L) . Now iref or i_L^* is compared with i_L . The duty cycle is maintained by the result of the comparator. The clock period and the value of the inductor are so chosen that the inductor current never falls to zero.

Fig. 2: Boost PFC ac-dc regulator under fixed-frequency Current Mode Control.

Depending upon the block diagram we design the above model and derived the several expressions [2,3,4,6] which are given below.

Supply system:

 v_{s}



Under normal operating conditions the supply system can be modelled as a sinusoidal voltage source of amplitude v_m and frequency f_s . The instantaneous voltage is:

$$(t) = v_m \sin \omega t$$

where $\omega = 2pifs$ electrical radians/second and t is instantaneous time.

In some topologies, the input is rectified line voltage $v_d(t)$ which can be given as:

 $v_d(t) = |v_s(t)| = |v_m \sin \omega t|$ ⁽²⁾

From the sensed supply voltage, an input-voltage template u(t) is estimated for converter topologies with AC side inductor as:

$$u(t) = v_s(t)/v_m \tag{3}$$

The input-voltage template for converter topologies with a DC side inductor is obtained from:

$$u(t) = |vs(t)|/vm \tag{4}$$

3 STATE EQUATIONS FOR MODELLING OF PFC BOOST

Feedback controller:

PFC converters, like most power electronics systems, cannot function without feedback control. Fig.1 shows a block diagram of typical control scheme for PFC converters – the current mode control [3]. This control scheme ensures regulated DC output voltage at high input power factor. The output DC voltage regulator generates a current command, which is the amount of current required to regulate the output voltage to its reference value. The output of the DC voltage regulator is then multiplied with a template of input voltage to generate an input current reference. This current reference has the magnitude required to maintain the output DC voltage close to its reference value and has the shape and phase of the input voltage – an essential condition for high input power factor operation.

(i) Output voltage controller:

A proportional integral (PI) voltage controller is selected for zero steady-state error in DC voltage (rippled in nature) regulation. The output capacitor voltage v_{dc} (or v_o) is sensed and compared with the set reference voltage v_{ref} . The resulting voltage error $v_e(n)$ at the nth sampling instant is:

$$v_e(n) = v_{ref} - v_{dc}(n) \tag{5}$$

The output of the PI voltage regulator $v_o(n)$ at the nth sampling instant of the PI

controller will be:

$$v_o(n) = v_o(n-1) + k_p \{v_e(n) - v_e(n-1)\} + k_i v_e(n)$$
(6)

Here k_p and k_i are the proportional and integral gain constants, respectively. $v_e(n-1)$ is the error at the (n - 1)th sampling instant. The output of the controller $v_o(n)$ after limiting to a safe permissible value is taken as the amplitude of the input current reference A (Fig. 2).

(ii) Reference current controller:

The input voltage template u(t) obtained from the sensed supply voltage is multiplied by the amplitude of the input current reference A to generate a reference current. The instantaneous value of the reference current is given as:

$i_{L}^{*} = AB / C^{2}$				(7)	
			4.5	1	

where *B* is the input voltage template *u*(*t*) and *C* is the input voltage feed forward component obtained by low-pass filtering the sensed input voltage signal.

Semiconductor switches:

Semiconductor switches, Mosfet *S* and Diode *D* are modelled as pure ON-OFF switches. No snubbers or non-idealities in the switches are modelled.

Load:

The converters are modelled as resistive loads having resistance *R*.

Power circuit:

The power circuit is modelled by first-order differential equations describing the circuit behaviour.

CONVERTER

There are two states[1][5] of the circuit depending on whether

(1)

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the controlled switch is open or closed. When switch is closed, the current through the inductor rises and any clock pulse arriving during that period is ignored. The switch opens when reaches the reference current. When switch is open, the current falls. The switch closes again upon the arrival of the next clock pulse.

The State Equations during "ON" period	
$di_L/dt = V_{in}/L - (r_i * i_L)/L$	(8)
$dv_c/dt = -v_c/C(R + r_c)$	(9)

The State Equations during "OFF" period $di_L/dt = V_{in}/L - i_L^*(r_i + R^*r_c/(R + r_c))/L - v_c^*R/L(R + r_c)$

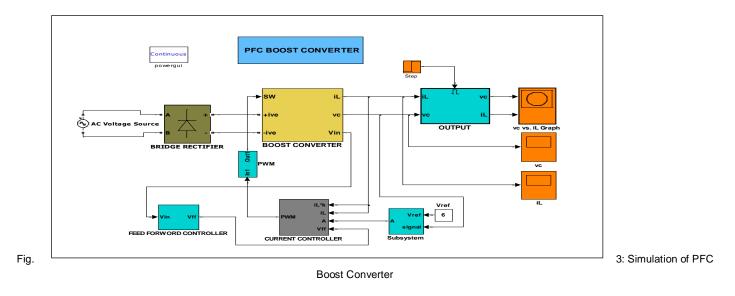
$$dv_c/dt = (R^*i_L - v_c)/C(R + r_c)$$
 (11)

where,

V _{in} =Input Voltage
L = Inductor
C = Capacitor
i _L = Inductor Current
v_c = Capacitor Voltage,
$r_i \& r_c$ = Parasitic Elements

SIMULATION OF PFC BOOST CONVERTER 4

Simulation of PFC Boost Converter is done by MATLAB 7.8R2009a. The model is totally designed by SimPowerSystem and Simulink blocks [3,4].



EXPERIMENTAL RESULTS 5

Here we are varying the value of Load Resistance R (in Fig.2) and we obtain the several periodic behavior of converter. Case I(Period I Operation)

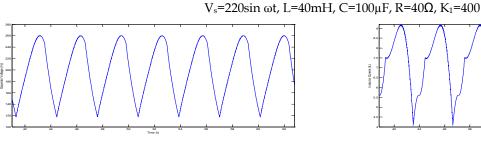


Fig.4(a) : O/P Voltage Waveform at Period I (R = 40 ohm)

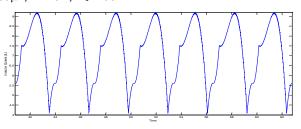


Fig.4(b) : Inductor Current Waveform at Period I (R = 40 ohm)

(10)

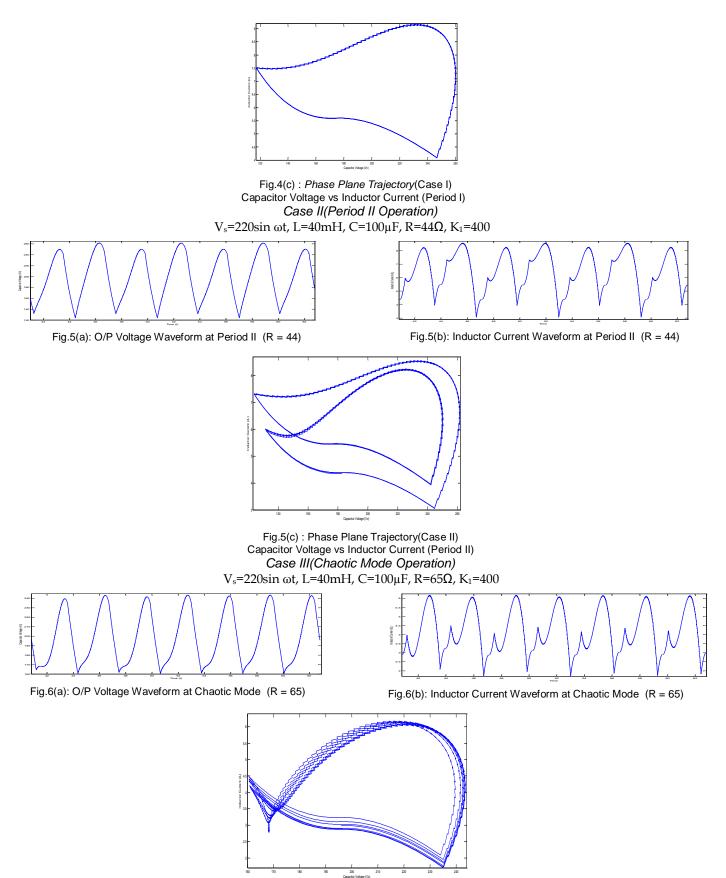


Fig.6(c) : Phase Plane Trajectory(Case III)

IJSER © 2012 http://www.ijser.org Capacitor Voltage vs Inductor Current (Chaotic Mode)

ANALYSIS OF EXPERIMENTAL RESULTS:

Here the state variables are inductor current (i_L) and capacitor voltage (v_c) .From above results we see that case I(Fig.4b) is operating at period I condition[7] and case II(Fig.5b) is operating at period II condition[7]. The output voltage waveform in Fig.5(a) is much more ripple free than Fig.4(a). We get better result of output voltage at same value of inductor (L) and capacitor (C), only changing the value of load resistance (R). The value of Capacitor(C) is chosen small just it operates as a boost converter. If we can increase more values of load resistance R, the system will operate at chaotic region and we can get better ripple free output voltage. This is the main observa-

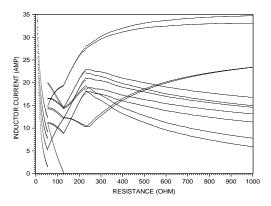


Fig.7(a):R vs iL (R is varied 1 to 1000ohm with step of 0.5)

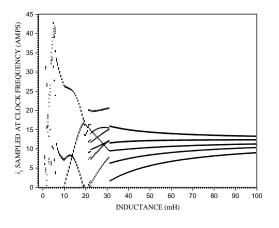


Fig.7(c):L vs i_L (L is varied 1 to 100mH with step of 0.5)

Analysis of Bifurcation Diagrams:

The above bifurcation diagrams are much more differ from other conventional bifurcation diagrams. In caonventional process the border [8] is fixed i.e. Iref (or i_L^*) is constant. In our experiment Iref (or i_L^*) is time varying natute i.e. order is time-varient. It is very difficult to analysis the bifurcation diagram properly. Actually the bifurcation is Period Doblling [7,6] in nature. The analysis is not given here. We are now working on analysis of diagrams.

tion that we get better output voltage profile at least value of capacitor. So, the investment is much more less than other conventional practical instruments.

6 **BIFURCATION DIAGRAMS**

Bifurcation diagrams are obtained from FORTRAN and ORIGIN 5.0 software. The data files are obtained after executing the FORTRAN programme of State Equations (8), (9), (10), (11) of PFC Boost Converter and iref equ (7). This data files are plotted by ORIGIN 5.0. Results are given below in Fig. 7(a), (b), (c), (d).

Bifurcation Diagrams

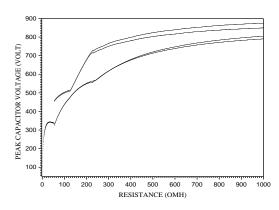


Fig.7(b):R vs Peak_ vc (R is varied 1 to 1000ohm with step of 0.5)

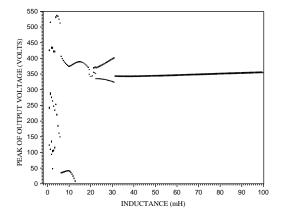


Fig.7(d):L vs Peak_ v_c (L is varied 1 to 100mH with step of 0.5)

7 CONTROL OF BIFURCATION

principle of control of bifurcations is based on perturbation or control by adding an extra input to the nonlinear dynamical system with the aim to modify its dynamics by stabilizing the desired behaviour. In our system, an extra Time Delayed Feedback action can be placed at any point of the voltage loop, for instance, at the output of the voltage controller.

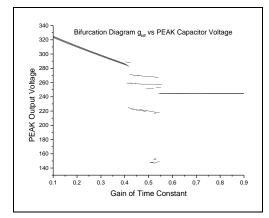
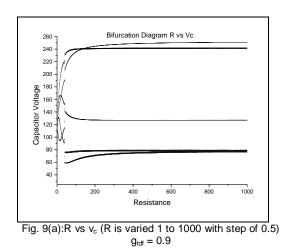


Fig.8: g_{tdf} vs Peak v_c (g_{tdf} is varied 0.1 to 0.9 with step of 0.01)

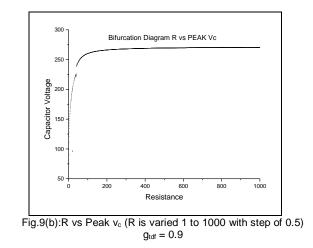
After Controlling Bifurcation Diagrams



From above figure (Fig. 8) we see that the stable value of v_c will be got after the value of $g_{tdf} = 0.6$. So, we assume the value of $g_{tdf} = 0.9$ and obtain the new bifurcation diagrams.

4 CONCLUSION

The boost PFC converter with continuous current mode control has been examined. Results highlight that the proposed model of practical pfc converter, experimental results and bifurcation diagrams. The value of load resistance is increased; the output capacitor voltage waveform is going to period I to period II and chaotic mode, that is the main cause of bifurcation. But the main benefit is the output voltage ripple is going less than the previous. Then the bifurcation control is implemented for obtaining stable operating zone. In а DC/DC converter system, the input voltage is constant and therefore the dynamical behavior is periodic with the switching frequency. On the other hand, the input voltage of the boost AC/DC PFC converter system is periodic with the line frequency. The results highlight that the dynamical behavior is periodic with the line frequency not with the switching frequency and simulation results are also agree with our statements.



If the Fig.7(b) will be compaired with Fig. 9(b), it will be shown the 2nd Fig. more stabler than 1st. It is possible only changing the bifurcation parameter i.e. bifurcation control.

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